REMARKS

Claims 1-18 are pending in the application, of which claim 1 is independent. Favorable reconsideration and further examination are respectfully requested.

The examiner has objected to the declaration for failing to comply with 37 C.F.R. 1.67(a). The applicant asks that this objection be held in abeyance.

The examiner has objected to the drawings for failing to comply with 37 C.F.R. 1.84(p)(4) because the reference character 16c in Fig. 1 has been used to designate both SDRAM and FlashRom. The applicant has amended Fig. 1.

The examiner has objected to the drawings for failing to comply with 37 C.F.R. 1.84(p)(5). The applicant has amended Figs. 2, 4, and 5.

The examiner has objected to the specification for informalities on page 5, page 12, and page 24. The applicant has amended the specification to obviate these objections. The examiner has also objected to the specification for the designation of "AMBA" in the drawings being referred to as "ASB" in the specification. It is the applicant's view that one of skill in the art would understand such designations in view of the specification. For example, page 8, lines 20-22 states "the ASB bus is a subset of the so called AMBA bus that is used with the Strong Arm Processor core."

The examiner objected to claims 2, 5, 9, 15, and 18 for informalitites. Claims 2, 5, 9, 15, and 18 have been amended to obviate these objections.

The examiner has rejected claims 12, 14, and 16 under 35 U.S.C. 112 as being indefinite for failing to point out and distinctly claim the subject matter the applicant regards as the invention. The applicant has amended claims 12, 14, and 16.

The Examiner rejected claims 1, 3, 9, and 10 under 35 U.S.C. 103(a) as being unpatentable over Callemyn (US 5,115,507) in view of Nakagawa (5,701,434).

Claim 1 relates to a controller for a random access memory. The controller includes an address and command queue that holds memory references from a plurality of microcontrol functional units, a first read/write queue that holds memory references from a computer bus, a second read/write queue that holds memory references from a core processor, and control logic

including an arbiter that detects the fullness of each of the queues and a status of outstanding memory reference to select a memory reference from one of the queues. Claim 1 is neither described nor suggested by Callemyn whether taken alone or in combination with Nakagawa.

Callemyn describes an arbitration unit for receiving requests from different processors and processing the requests based on whether the requests are for a single word or a plurality of words (see abstract). For example, in figures 1A and 1B the arbitration system receives requests from three processors: a display processor (DP), a graphics processor (GP), and a central processing unit (CPU). Callemyn does not describe or suggest receiving requests from devices other than the processors. Therefore, Callemyn does not disclose or suggest an arbitration unit that includes "an address and command queue that holds memory references from a plurality of microcontrol functional units, a first read/write queue that holds memory reference from a computer bus, a second read/write queue that holds memory references from a core processor" as recited in the applicant's claim 1.

In addition, as conceded by the examiner, Callemyn does not disclose that "the modules or registers for holding memory references are set up as queues" (see office action page 8). Nakawa discloses a single queue for holding all requests from multiple sources. Nakawa describes the advantage of such a single queue system as "reducing the scale of a random access queue as compared with the scale of a conventional access queue for each bank." Nakawa does not disclose or suggest using multiple queues in the applicant's claim 1 that includes an "address and command queue," "a first read/write queue," and "a second read/write queue." Therefore, even if one were to combine system of Callemyn with the single queue of Nakawa, it would not have made obvious the applicant's claim 1.

For at least the same reasons, applicant submits claim 1 should be allowed, applicant submits that dependent claims 2-4, 9-11, and 13-18 should be allowed.

The applicant respectfully acknowledges the allowable subject matter of claims 5-8 and 12-13.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or

concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Enclosed is a check for the Petition for Extension of Time fee. Please apply any other

Respectfully submitted,

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